Ordering number : EN4896

Monolithic Linear IC

No. 4896

SANYO

LA7256

High-Fidelity Audio Signal Record/Playback Processing Circuit for VCR Products

Overview

The LA7256 provides the record and playback amplification functions required for high-fidelity audio signal processing in VCR systems. The record system supports S-VHS and over-recording, and also supports the provision of an adjustment-free record current by using a constant-current regulated output scheme incorporating an AGC circuit. The playback system consists of a high-gain preamplifier with a small DC offset, and includes a built-in EP gain increasing function.

Functions

- Preamplifier (two channels)
- RF switching between CH1 and CH2
- Record AGC amplifier (for over-recording and S-VHS)
- Constant-current regulated output record amplifier
- Buffer amplifier that can be used in both record and playback

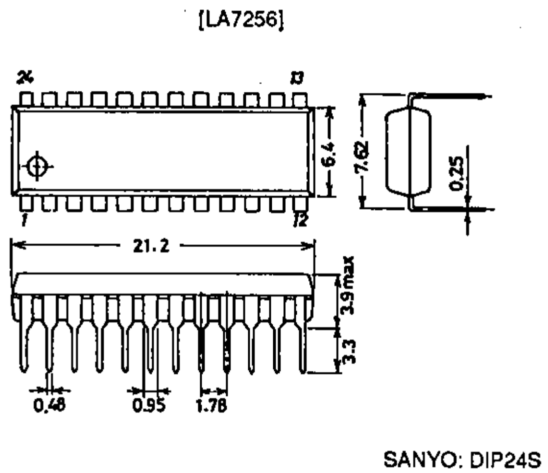
Features

- Minimal number of required external components
- The playback amplifier output DC offset is small.
- Built-in EP mode gain emphasis
- Record AGC that handles three modes (for an adjustment-free record current)
- Built-in buffer amplifier that can be used to construct an active filter.

Package Dimensions

unit: mm

3067-DIP24S



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Allowable power dissipation	Pd max	Ta ≤ 65°C	700	mW
Operating temperature	Topr		–10 to +65	°C
Storage temperature	Tstg		–55 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5.0	V
Operating supply voltage range	V_{CC} op		4.5 to 5.5	V

Operating Characteristics at Ta = 25°C, V_{CC} = 5 V, in the specified test circuit

Parameter	Symbol	Conditions	min	typ	max	Unit
[Playback Mode]						
Circuit current	I_{CCP}	No input: the pin 14 influx current	13	18	23	mA
Voltage gain, CH1	G_{VP1}	Pin 20 input = 100 µVp-p, f = 1.5 MHz, pin 1 = low: measure the pin 3 output.	72.5	75.5	78.5	dB
Voltage gain, CH2	G_{VP2}	Pin 17 input = 100 µVp-p, f = 1.5 MHz, pin 1 = high: measure the pin 3 output.	72.5	75.5	78.5	dB
Voltage gain difference	ΔG_{VP}	$G_{VP1} - G_{VP2}$	–2	0	+ 2	dB
EP gain emphasis	ΔG_{EP}	Pin 20 input = 100 µVp-p, f = 1.5 MHz, pin 1 = low: the ratio of the pin 3 outputs when pin 2 is high/low	1.7	2.4	3.1	dB
Frequency characteristics, CH1	f_{P1}	Pin 20 input = 100 µVp-p, pin 1 = low: the difference in the levels on pin 3 when f = 2.2 MHz and 1.0 MHz	–3.0	–1.0	0	dB
Frequency characteristics, CH2	f_{P2}	Pin 17 input = 100 µVp-p, f = 1.5 MHz, pin 1 = high: the difference in the levels on pin 3 when f = 2.2 MHz and 1.0 MHz	–3.0	–1.0	0	dB
Crosstalk CH1 to CH2	$CT_{1 \to 2}$	Pin 17 input = 0, pin 20 input = 100 µVp-p, f = 1.5 MHz: the difference in the pin 3 output levels when pin 1 goes from low to high		–40	–35	dB
Crosstalk CH2 to CH1	$CT_{2 \to 1}$	Pin 20 input = 0, pin 17 output = 100 µVp-p, f = 1.5 MHz: the difference in the pin 3 output levels when pin 1 goes from high to low		–40	–35	dB
Equivalent input noise voltage CH1	V_{NP1}	With pin 20 grounded through 0.01 µF and 1 Ω, pin 1 = low: the pin 3 noise in input equivalent*1		0.8	1.0	µVrms
Equivalent input noise voltage CH2	V_{NP2}	With pin 17 grounded through 0.01 µF and 1 Ω, pin 1 = high: the pin 3 noise in input equivalent*1		0.8	1.0	µVrms
Second harmonic distortion CH1	$2THD_1$	Pin 20 input = 100 µVp-p, f = 1.5 MHz, pin 1 = low: the second harmonic in the pin 3 output		–50	–40	dB
Second harmonic distortion CH2	$2THD_2$	Pin 17 input = 100 µVp-p, f = 1.5 MHz, pin 1 = high: the second harmonic in the pin 3 output		–50	–40	dB
Maximum output voltage CH1	V_{OMP1}	With the pin 20 input varying, f = 1.5 MHz, pin 1 = low: when the pin 3 third harmonic distortion is –30 dB	2.0			Vp-p
Maximum output voltage CH2	V_{OMP2}	With the pin 17 input varying, f = 1.5 MHz, pin 1 = high: when the pin 3 third harmonic distortion is –30 dB	2.0			Vp-p
Output DC offset 1	ΔV_{ODC1}	Pin 17 and 20 inputs = 0, pin 1 = low, pin 2 = low (SP): the difference in the pin 3 DC level when pin 1 goes from low to high	–30	0	+30	mV
Output DC offset 2	ΔV_{ODC2}	Pin 17 and 20 inputs = 0, pin 1 = low, pin 2 = high (EP): the difference in the pin 3 DC level when pin 1 goes from low to high	–50	0	+50	mV
Head switching: CH1 hold voltage	V_{HS1}	The pin 1 DC voltage required to operate CH1	0		1.0	V
Head switching: CH2 hold voltage	V_{HS2}	The pin 1 DC voltage required to operate CH2	3.0		V_{CC}	V
Playback mode switch on resistance	R_{SW}	Calculate from the voltage difference on pin 16 when the pin 16 influx current is 1 mA and 2 mA.		4.0	6.0	Ω
SP hold voltage	V_2SP	The pin 2 voltage required to hold SP mode	0		1.0	V
EP hold voltage	V_2EP	The pin 2 voltage required to hold EP mode	3.0		V_{CC}	V
PB hold voltage	V_{5L}	The pin 5 voltage required to hold PB mode	0		1.0	V
[Record Mode]						
Circuit current	I_{CCR}	No signal, the pin 14 influx current	45	63	81	mA
Output current	I_{OR}	Pin 9 input = 180 mVp-p, f = 1.5 MHz: measure the pin 16 output	48	53	58	mAp-p
AGC control characteristics 1	ΔV_{AGC1}	Pin 9 input = 90 and 180 mVp-p, f = 1.5 MHz: the ratio of the pin 16 output levels	–0.5	–0.2		dB
AGC control characteristics 2	ΔV_{AGC2}	Pin 9 input = 360 and 180 mVp-p, f = 1.5 MHz: the ratio of the pin 16 output levels		0.2	0.5	dB
Cross modulation distortion 0.4 MHz component	CMD_{04}	For a pin 9 input*2, the 0.4 MHz spurious signal in the pin 16 output current			–40	dB
Cross modulation distortion 0.9 MHz component	CMD_{09}	For a pin 9 input*2, the 0.9 MHz spurious signal in the pin 16 output current			–40	dB

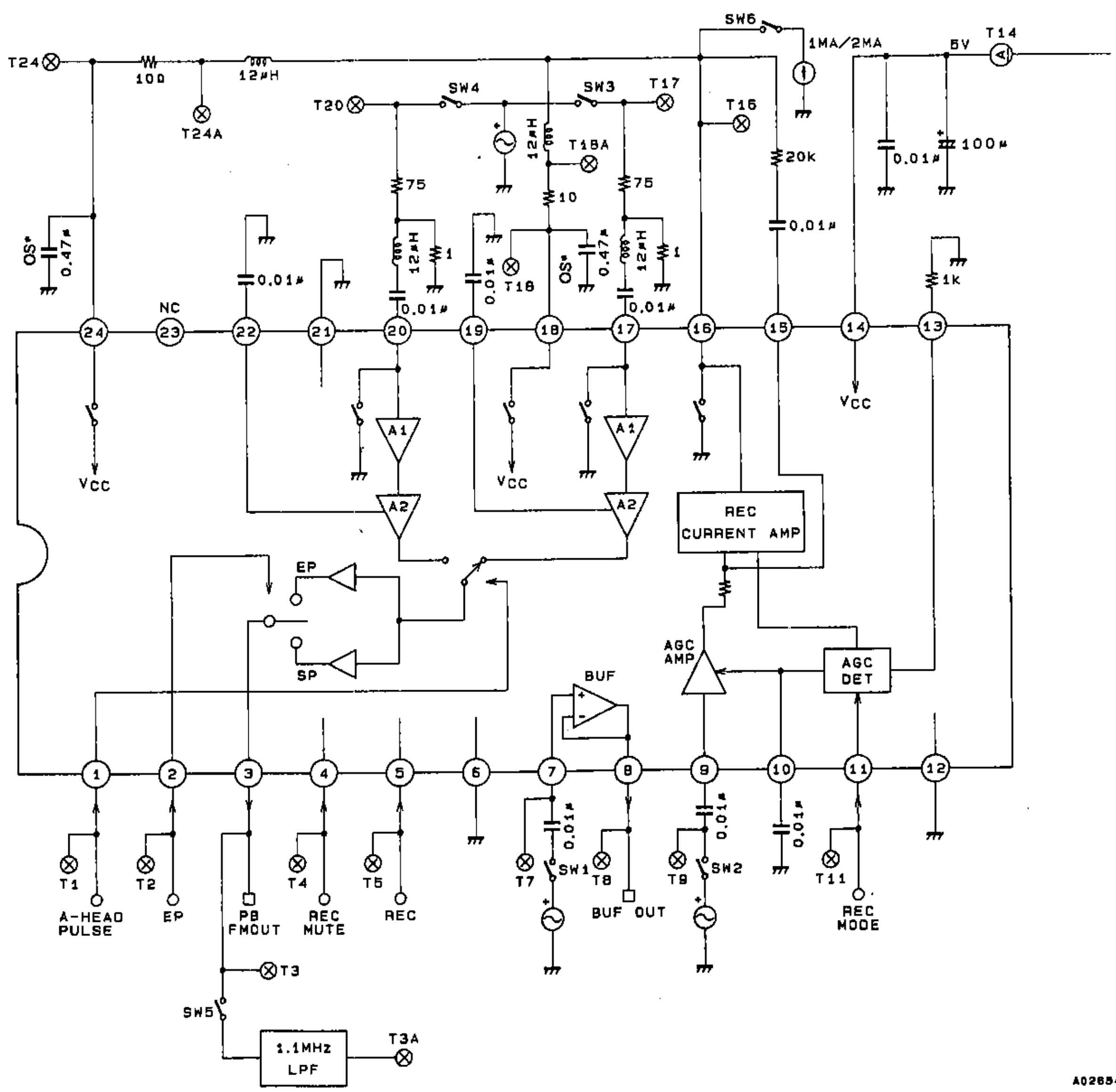
Note: 1. Measure the input noise voltage after passing the pin 3 output (playback FM output) through a 1.1 MHz low-pass filter.
2. 1.3 MHz (70 mVp-p) + 1.7 MHz (180 mVp-p)

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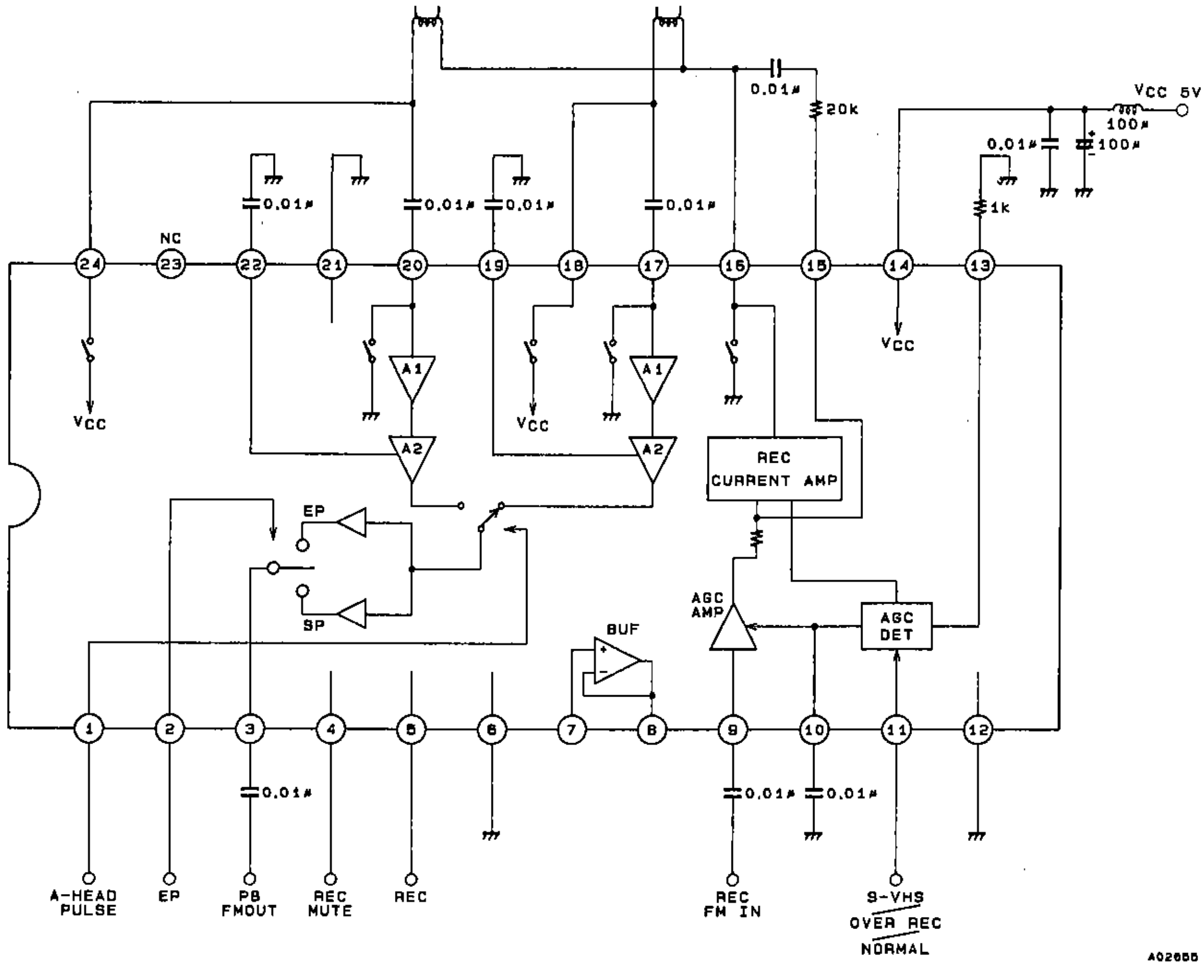
Parameter	Symbol	Conditions	min	typ	max	Unit
Over-record hold voltage	V_{11M}	The pin 11 DC voltage for over-record mode	1.5		3.0	V
Over-record current ratio	$I_{O\text{-}OV}$	Pin 9 input = 180 mVp-p, f = 1.5 MHz, pin 11 = middle level: measure the pin 16 output current	1.7	2.2	2.7	dB
S-VHS hold voltage	V_{11H}	The pin 11 DC voltage for S-VHS mode	3.5		V_{CC}	V
S-VHS current ratio	$I_{O\text{-}SV}$	Pin 9 input = 180 mVp-p, f = 1.5 MHz, pin 11 = high: measure the pin 16 output current	–2.0	–2.6	–3.2	dB
Record mute hold voltage 1	V_{4L}	The pin 4 DC voltage when record muting is off	0		1.0	V
Record mute hold voltage 2	V_{4H}	The pin 4 DC voltage when record muting is on	3.0		V_{CC}	V
Mute attenuation	I_{OR}, M_U	Pin 9 input = 180 mVp-p, f = 1.5 MHz, pin 4 = high: measure the pin 16 output current			–40	dB
Record hold voltage	V_{5H}	The pin 5 voltage required to hold record mode	3.0		V_{CC}	V
[Built-in Buffer]						
Buffer I/O DC offset	ΔV_{BUF}		–10		+10	mV
Buffer frequency characteristics	f_{BUF}	Pin 9 input = 180 mVp-p, f = 1/10 MHz	–1		+1	dB

Test Circuit Diagram



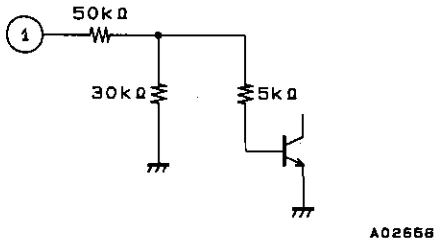
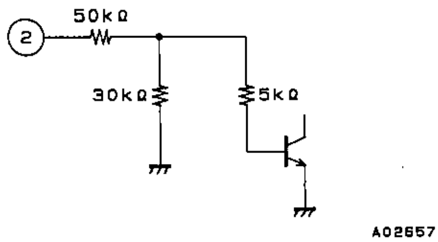
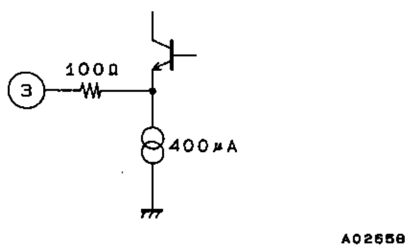
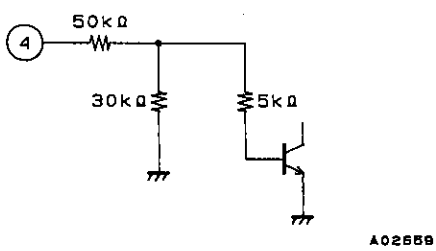
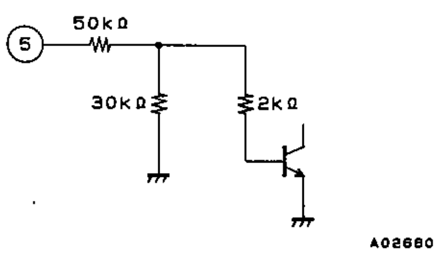
Unit (resistance: Ω, capacitance: F)
*: Organic Semiconductor

Application Circuit Block Diagram



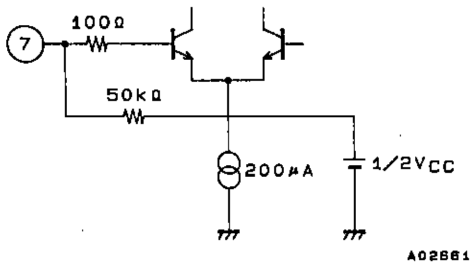
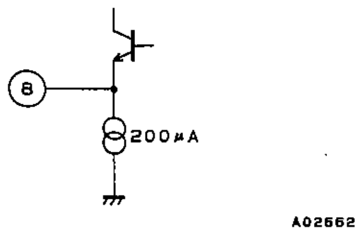
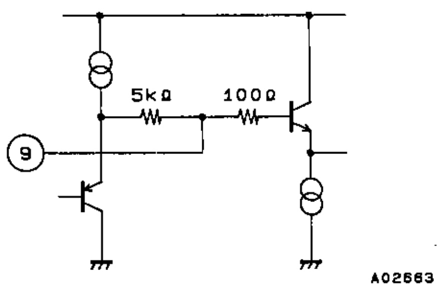
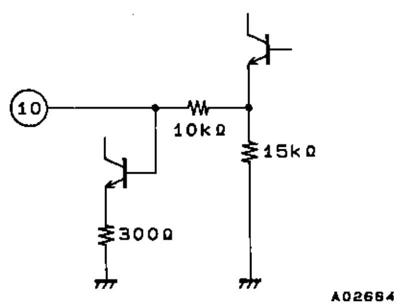
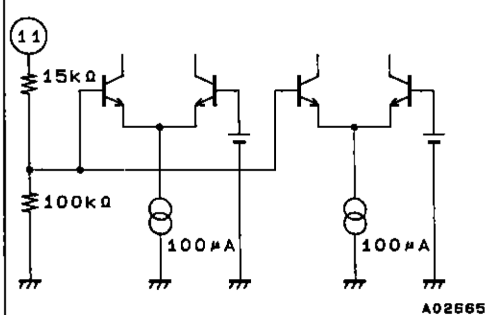
Unit (resistance: Ω, capacitance: F)

Pin Functions

Pin No.	Symbol	Pin internal equivalent circuit	Function
1	A-HEAD PULSE		Low: 0 to 1.0 V → CH1 High: 3.0 to V_{CC} → CH2
2	ES/SP		Low: 0 to 1.0 V → SP High: 3.0 to V_{CC} → EP
3	PB-FM OUT		
4	REC MUTE		Low: 0 to 1.0 V → Mute off High: 3.0 to V_{CC} → Mute on
5	REC		Low: 0 to 1.0 V → PB High: 3.0 to V_{CC} → REC
6	GND		Ground for the playback output stage and record circuits

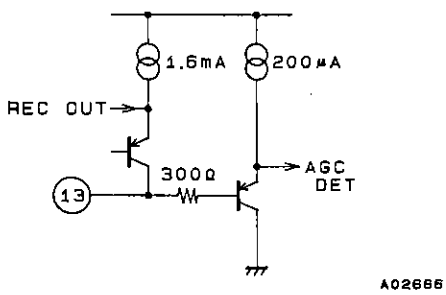
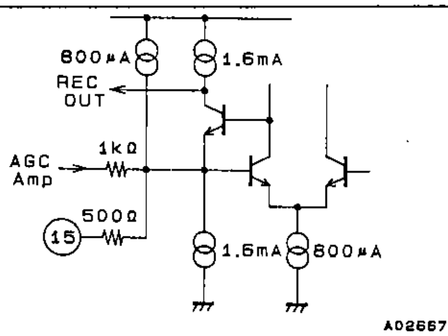
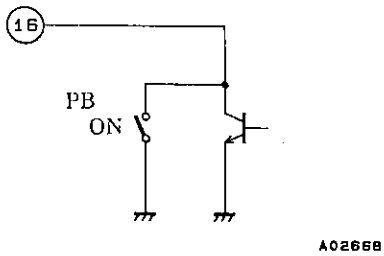
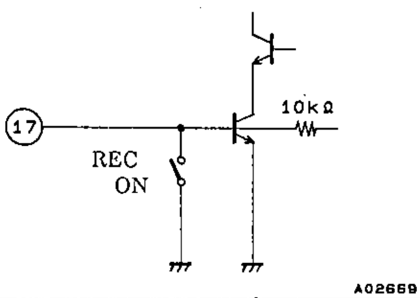
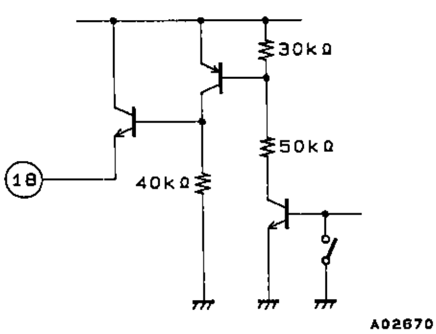
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Pin No.	Symbol	Pin internal equivalent circuit	Function
7	BUFF IN		
8	BUFF OUT		DC voltage = 1/2 V_{CC}
9	REC FM IN		Record amplifier input
10	AGC FILT		Detects the record amplifier AGC detector output
11	REC MODE		Low: 0 to 1.0 V → Normal Middle: 1.5 to 3.0 V → Over-record High: 3.5 V to V_{CC} → S-VHS
12	REC OUT GND		Ground for the record output circuits

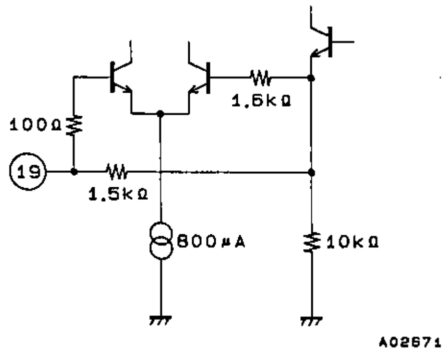
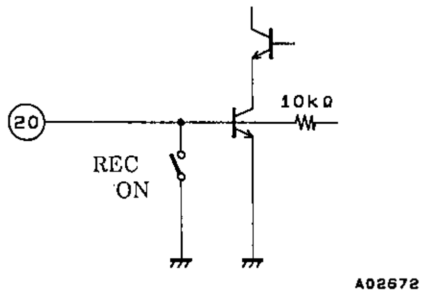
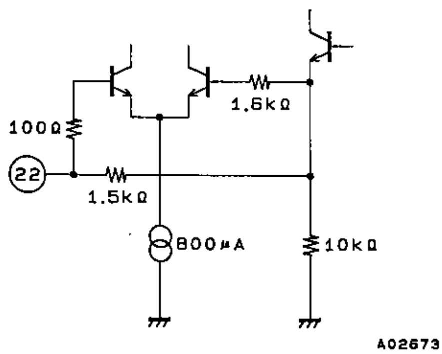
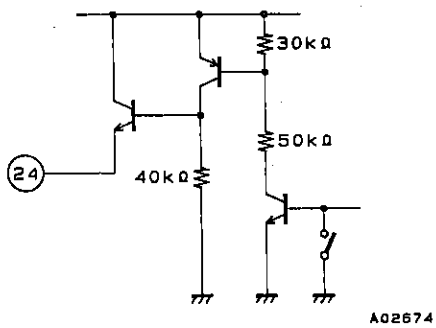
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Pin No.	Symbol	Pin internal equivalent circuit	Function
13	REC-CURR-ADJ		Converts the record output current output to a voltage.
14	V_{CC}		
15	REC BIAS		Input block for the record current amplifier
16	REC OUT		Switch for record current output and playback mode on On in PB mode
17	CH2-IN		Playback amplifier CH2 input
18	PSW2		CH2 head current supply

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Pin No.	Symbol	Pin internal equivalent circuit	Function
19	FILT2		Generates the playback amplifier CH2 DC bias.
20	CH1-IN		Playback amplifier CH1 input
21	PB GND		Ground for the playback amplifier
22	FILT1		Generates the playback amplifier CH1 DC bias.
23	NC		
24	PSW1		Record amplifier CH2 head current supply

This catalog provides information as of June, 1995. Specifications and information herein are subject to change without notice.